

PATENT
IBM Docket No. RAL9-2000-0057US1

Amendments to the Specification:

On page 9, paragraph 23, line 27, please change "at 171 in Figure 1" to "at 171 in Figure 2.":

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In accordance with important distinguishing characteristics of this invention, a non-blocking switch fabric is provided within the computer system 100 so as to be interposed between and among the CPU 110 and those elements of the system 100 which together provide and/or directly access the system memory. The switch fabric preferably is provided by a network processor, functioning either with or without an associated secondary switch fabric. The network processor may be integrated into the computer system 100 as indicated ~~at 171 in Figure 1~~ at 171 in Figure 2. By so implementing the incorporation of a network processor into the system, benefits are gained in terms of performance by providing dedicated, full duplex links from the processor 171 to each of the subsystems. These subsystems can include volatile memory elements 172, non-volatile memory elements 174, interface devices such as a network interface 175, and other input/output devices such as a keyboard or display 176. By placing memory address translation, data pipelining and caching within the hardware provided by the processor 171, cycles of the CPU 110 are freed to more efficiently exercise application software. By implementing these memory control functions with a hardware assist, multiple simultaneous operations can be executed in parallel, where (by way of contrast) a software implementation executes only one task at a time. The dynamic nature of memory management, with address spaces being continuously created, modified and deleted, forces each address translation to synchronize any processors executing the software implementation in order to avoid conflicts among such processors as they access memory.
